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10/572,577	03/17/2006	Kazuhiko Ikeda	L9289.06127	2535

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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,577	IKEDA ET AL.	
	Examiner	Art Unit	
	LAWRENCE B. WILLIAMS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendments filed on 3/31/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The indicated allowability of claims 1-11 is withdrawn in view of the newly discovered reference(s) to Eisenberg et al. (US Patent 6,452,446 B1), Ishida et al. (US 2003/0016081 B1) and Ocenasek et al. (US Patent 6,674,324 B1). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2-6, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenberg et al. (US Patent 6,452,446 B1) in view of Ishida et al (US 2003/0016081 B1).

(1) Regarding claim 1, Eisenberg et al. discloses in Fig. 2, an amplifier circuit comprising: a constant envelope signal generating section (element 16, 50, 50 are vector modulators which produce constant envelope signal) for generating a plurality of constant envelope signals from an input signal (RF Input); a pilot signal generating section (element 24, pilot signal generator two pilot signals for the two constant envelope signals) for generating a plurality of pilot signals associated with the generated plurality of constant envelope signals, respectively, the plurality of pilot signals having predetermined amplitudes, predetermined phases, respectively, said phases being different from each other (col. 7, lines 8-14; Eisenberg et

al. teaches equal amplitude of the pilot signals an that they are mutually antiphase (phases different). A predetermined frequency of the pilot signals would be inherent feature); an addition section (couplers, 22, CPLR 7) for adding the plurality of pilot signals to the generated plurality of constant envelope signals; an amplifying section (amplifier 20, amplifier 80) for amplifying the plurality of constant envelope signals to which the plurality of pilot signals are added; and a correction section (Output power balance control loop, 117 using elements 51 (amplitude), 53 (phase) and Output distortion power minimization mechanism, 110 using elements 71 (amplitude)and element 70 (phase) for correcting an amplitude or phase of one of the generated plurality of constant envelope signals using a signal component included in the amplified plurality of constant envelope signals and corresponding to the plurality of pilot signals.

Eisenberg et al. does not explictly disclose the generated pilot signals having frequencies different from each other.

However, Ishida et al. discloses a method of controlling an amplifier wherein he teaching generating a plurality of pilot signals with frequencies being different from each other (pg. 2, paragraph [0013]).

One of ordinary skill in the art at the time of invention would have been motivated to incorporate the teachings of Ishida et al. as of optimizing the removal or suppression of distortion.

(2) Regarding claim 2, Eisenberg et al. also discloses wherein the pilot signal generating section generates the plurality of pilot signals which are sine wave signals (Fig. 24 discloses an oscillator for generating the pilot signals inherently implying sine wave signals).

(3) Regarding claim 3, Eisenberg et al. also discloses wherein the pilot signal generating section generates the plurality of pilot signals in such a manner that amplitudes are equal to each other (col. 7, lines 8-14).

(4) Regarding claim 4, Ishida et al. also discloses wherein the pilot signal generating section generates the plurality of pilot signals having the frequencies outside a frequency band of the input signal (pg. 2, paragraph [0013]).

One of ordinary skill in the art at the time of invention would have been motivated to incorporate the teachings of Ishida et al. as of optimizing the removal or suppression of distortion.

(5) Regarding claim 5, Eisenberg et al. also discloses the amplifier circuit according to claim I, further comprising a combining section (Fig. 3, element 90) for combining the plurality of constant envelope signals to which the plurality of pilot signals are added, wherein the pilot signal generating section generates the plurality of pilot signals which cancel each other out when combining is performed by the combining section (col. 7, lines 11-14).

(6) Regarding claim 6, Eisenberg et al. also discloses the amplifier circuit according to claim 1, wherein the pilot signal generating section generates the plurality of pilot signals including a first pilot signal and second pilot signal which have opposite phases to each other (col. 7, lines 8-9).

(7) Regarding claim 9, Ishida et al. also discloses a wireless base station apparatus comprising the amplifier circuit of claim 1 (pg. 1, paragraph [0004]).

One of ordinary skill in the art would have been motivated to incorporate the teachings as a method of optimization of the amplifier at the base station.

(8) Regarding claim 10, Ishida et al. also discloses a terminal apparatus comprising the amplifier circuit of claim 1 (pg. 1, paragraph [0004]).

One of ordinary skill in the art would have been motivated to incorporate the teachings as a method of optimization of the amplifier at the wireless terminal apparatus.

(9) Regarding claim 11, Eisenberg et al. discloses in Fig. 2, an amplifying method in a wireless transceiver apparatus (pg. 1 paragraph [0004] discloses a base station), the amplifying method comprising the steps generating, by a constant envelope signal generating section (element 16, 50, 50 are vector modulators which produce constant envelope signal) a plurality of constant envelope signals from an input signal (RF Input); generating a plurality of pilot signals (element 24, pilot signal generator two pilot signals for the two constant envelope signals) associated with the generated plurality of constant envelope signals, respectively, the plurality of pilot signals having predetermined amplitudes, predetermined phases, respectively, said phases being different from each other (col. 7, lines 8-14; Eisenberg et al. teaches equal amplitude of the pilot signals an that they are mutually antiphase (phases different). A predetermined frequency of the pilot signals would be inherent feature); adding the plurality (couplers, 22, CPLR 7) of pilot signals to the generated plurality of constant envelope signals; amplifying (amplifier 20, amplifier 80) the plurality of constant envelope signals to which the plurality of pilot signals are added; and correcting (Output power balance control loop, 117 using elements 51 (amplitude), 53 (phase) and Output distortion power minimization mechanism, 110 using elements 71 (amplitude)and element 70 (phase)) an amplitude or phase of one of the generated plurality of constant envelope signals using a signal component included in the amplified plurality of constant envelope signals and corresponding to the plurality of pilot signals.

Eisenberg et al. does not explictly disclose the generated pilot signals having frequencies different from each other.

However, Ishida et al. discloses a method of controlling an amplifier wherein he teaching generating a plurality of pilot signals with frequencies being different from each other (pg. 2, paragraph [0013]).

One of ordinary skill in the art at the time of invention would have been motivated to incorporate the teachings of Ishida et al. as of optimizing the removal or suppression of distortion.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenberg et al. (US Patent 6,452,446 B1) in view of Ishida et al (US 2003/0016081) B1 as applied to claim 1 above, and further in view of Ocenasek et al. (US Patent 6,674,324 B1).

Claim 8 inherits all limitations of claim 1. As noted above, the combination of Eisenberg et al. and Ishida et al. disclose all limitations of claim 1 above. They do not teach a frequency characteristic correction section for correcting a frequency characteristic of one of the generated plurality of signals using a signal component included in the amplified plurality of signals and corresponding to the plurality of pilot signals.

However, Ocenasek et al. discloses an amplifier distortion reduction system wherein he teaches an amplifier circuit according to claim 1, further comprising a frequency characteristic correction section for correcting a frequency characteristic of one of the generated plurality of signals using a signal component included in the amplified plurality of signals and corresponding to the plurality of pilot signals (col. 6, lines 53-67; Ocenasek et al. discloses the

control circuitry 94 providing signals to produce gain, phase and or equalization (correcting a frequency characteristic by using injected pilot signals (Fig. 1)).

One of ordinary skill in the art at the time of invention would have been motivated to incorporate the teachings of Ocenasek et al. to allow amplifier distortion reduction which adapts to changing operating conditions, such as changes in input signals(s), temperature and/or component performance (col. 6, lines 60-67).

Allowable Subject Matter

5. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Yoshikawa et al. discloses in US Patent 5,691,668 Feedforward Amplifier, an amplifier circuit with a first and second pilot signal source.

b.) Eisenberg et al. discloses in US 2002/0084845 A1 Closed Loop Active Cancellation Technique (ACT)-Based RF Power Amplifier Linearization Architecture, an amplifier with injected pilot tone.

c.) Nakayama et al. discloses in US 2002/0105379 A1 Feedforward Amplifier, an amplifier with first and second pilot signal generating means.

d.) Myer discloses in US Patent 7,035,312 B2 Pilot Signal Cycling Technique For A Control System That Reduces Distortion Produced By Electrical Circuits.

e.) Ishida et al. discloses in US Patent 6,750,706 B2 Control Method And Circuit For Feedforward Distortion Compensation Amplifier, wherein he teaches a first and second pilot signal obtained from a first and second pilot signal source are inserted into the input signal or output signal from a main amplifier.

f.) Nitz et al. discloses in US Patent 6,496,062 B1 Predistortion System And Method Using A Pilot Signal wherein he teaches using a pilot signal to determine a predistortion function which is used to produce amplitude and/or phase adjustments.

g.) Ishigami et al. discloses Feedforward Amplifier in US 2004/0017253 A1 where he teaches using a first and second pilot signal.

h.) Suzuki et al. discloses Feed-forward Amplifier in US Patent 6,392,483 B2.

i.) Suzuki et al. discloses Feed-forward Amplifier in US Patent 6,320,464 B1.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tesfaldet Bocure/
Primary Examiner, Art Unit 2611

lbw
June 24, 2009